CONTROL OF SIMULTANEOUS SWITCH NOISE FROM MULTIPLE OUTPUTS

FIELD OF THE INVENTION

[0001] The present invention relates to a method and apparatus for reducing the transient currents associated with simultaneously switched outputs of a semiconductor chip.

RELATED ART

[0002] Output signals of a semiconductor chip are typically switched simultaneously in response to an output clock signal. Such simultaneously switched outputs result in large transient currents, which cannot be easily controlled. Conventional methods used to control the large transient currents associated with simultaneously switched outputs include controlling the slew rate of the output signals and/or controlling the strength of the output signals. However, such methods either require excessive circuitry, or reduce the integrity of the output signals.

[0003] It would therefore be desirable to have an improved method and apparatus for reducing the high transient current associated with simultaneously switched outputs.

SUMMARY

[0004] Accordingly, the present invention reduces transient current created during output switching by time multiplexing the output switching operation within each clock period. A plurality of output clock signals are generated in response to an input clock signal, wherein the output clock signals are phase-shifted with respect to the input clock signal. Each of the phase-shifted clock signals exhibits an active (e.g., rising) edge during a single period of the input clock signal. Different groups of input/output blocks are switched in response to the various phase-shifted clock signals, such that output switching occurs at various times during the period of the input clock signal. The phase-shifted clock signals can be generated with predetermined

phase differences or with dynamically determined phase differences.

[0005] In accordance with one embodiment, a digital clock manager generates a plurality of output clock signals, which are separated by 90-degree phase differences. For example, a first output signal may be synchronous with the input clock signal, a second output clock signal may lag the first output clock signal by 90 degrees, a third output clock signal may lag the second output clock signal by 90 degrees, and a fourth output clock signal may lag the third output clock signal by 90 degrees. A first set of input/output resources are clocked by the first output clock signal, a second set of input/output resources are clocked by the second output clock signal, a third set of input/output resources are clocked by the third output clock signal, and a fourth set of input/output resources are clocked by the fourth output clock signal. As a result, the transient switching current existing at any given time is reduced by a factor of four.

[0006] In accordance with another embodiment, a digital clock manager determines the period of the input clock signal. For example, delay elements may be introduced to the path of the input clock signal until the resulting output clock signal is synchronous with the input clock signal. At this time, the delay introduced by the delay elements is equal to one period of the input clock signal. The input clock signal (or resulting output clock signal) is applied to a chain of series-connected programmable delay lines, thereby generating a corresponding plurality of delayed clock signals. The delay introduced by each of the programmable delay lines is selected with respect to the period of the input clock signal. Thus, the sum of the delays introduced by the programmable delay lines is less than the period of the input clock signal.

[0007] In one embodiment, each of the programmable delay lines includes a plurality of delay elements, wherein each of the delay elements in the programmable delay lines is

identical to each delay element in the digital clock manager. In this embodiment, the number of delay elements enabled within each of the programmable delay lines is determined by dividing the number of delay elements introduced by the digital clock manager by the number of programmable delay lines. As a result, each of the programmable delay lines introduces the same delay to the received clock signal.

[0008] The present invention will become more clearly understood in view of the following description and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Fig. 1 is a block diagram of a field programmable gate array (FPGA) in accordance with one embodiment of the present invention.

[0010] Fig. 2 is a waveform diagram illustrating an input clock signal CLK_{IN}, associated data values, and output clock signals CLK_0, CLK_{90}, CLK_{180} and CLK_{270}, in accordance with one embodiment of the present invention illustrated by Fig. 1.

[0011] Fig. 3 is a circuit diagram illustrating a portion of an FPGA in accordance with another embodiment of the present invention.

[0012] Fig. 4 is a circuit diagram of a programmable delay line in accordance with one embodiment of the present invention illustrated by Fig. 3.

[0013] Fig. 5 is a waveform diagram illustrating an input clock signal CLK_{IN}, output clock signals CLK_0-CLK_{16} and associated data values in accordance with one embodiment of the present invention illustrated by Fig. 3.

DETAILED DESCRIPTION

[0014] Fig. 1 is a block diagram of a semiconductor chip 100 in accordance with one embodiment of the present invention. In the described embodiments, semiconductor chip 100 is a programmable logic device, such as a field programmable gate array (FPGA). However, semiconductor chip

100 need not be a programmable logic device. FPGA 100 includes an array of configurable logic blocks (CLBs) and a programmable interconnect structure, which are illustrated as block 101, a digital clock manager (DCM) 111, and configurable input/output blocks (IOBs) 121-124, 131-134, 141-144 and 151-154. In general, the elements of FPGA 100 are largely conventional, and are described in more detail in "Virtex™-II Platform FPGA Handbook", available from Xilinx, Inc. As described in more detail below, the configuration of FPGA 100 significantly reduces transient currents during output switching.

[0015] FPGA 100 operates as follows in accordance with one embodiment of the present invention. First, FPGA 100 is configured to implement a desired circuit by programming configuration memory cells of the FPGA. DCM 111 is configured to provide four output clock signals CLK_0, CLK_{90}, CLK_{180} and CLK_{270} in response to an input clock signal CLK_{IN} during normal operation of FPGA 100. Although DCM 111 generates four clock phases in the present embodiment, it is understood that DCM 111 can be modified to provide other numbers of clock phases in other embodiments.

[0016] Fig. 2 is a waveform diagram illustrating the input clock signal CLK_{IN}, associated data values D1-D4, and the clock signals CLK_0, CLK_{90}, CLK_{180} and CLK_{270}. As illustrated by Fig. 2, the clock signals CLK_0, CLK_{90}, CLK_{180} and CLK_{270} are separated in phase by ninety degrees. In the described embodiment, the input clock signal CLK_{IN} and the clock signal CLK_0 are synchronized by DCM 111. Thus, both the CLK_{IN} and CLK_0 signals exhibit rising edges at time T_0. One-quarter period later, at time T_1, the CLK_{90} signal exhibits a rising edge, such that the CLK_{90} signal lags the CLK_0 signal by 90 degrees. One-quarter period after time T_1 (at time T_2), the CLK_{180} signal exhibits a rising edge, such that the CLK_{180} signal lags the CLK_{90} signal by 90 degrees. One-quarter

period after time T_2 (at time T_3), the CLK_{270} signal exhibits a rising edge, such that the CLK_{270} signal lags the CLK_{180} signal by 90 degrees. Note that data values D1[15:0] are clocked out of FPGA 100 during the clock period that includes times T_0-T_3.

[0017] In accordance with one embodiment, various IOBs of FPGA 100 are clocked with different clock signals. For example; IOBs 121-124 are clocked with the CLK_0 signal, IOBs 131-134 are clocked with the CLK_{90} signal, IOBs 141-144 are clocked with the CLK_{180} signal, and IOBs 151-154 are clocked with the CLK_{270} signal. Thus, four bits of the D1[15:0] value (e.g., D1[3:0]) are clocked out through IOBs 121-124 at time T_0, four bits of the D1[15:0] value (e.g., D1[7:4]) are clocked out through IOBs 131-134 at time T_1, four bits of the D1[15:0] value (e.g., D1[11:8]) are clocked out through IOBs 141-144 at time T_2, and four bits of the D1[15:0] value (e.g., D1[15:2]) are clocked out through IOBs 151-154 at time T_3. Thus, only one fourth of the IOBs are clocked at any given time. This substantially reduces the transient current associated with output switching. Although the clock signals are applied to adjacent IOBs in an interleaved manner in the illustrated example, this is not required. For example, each of the IOBs located along a single edge of FPGA 100 (e.g., IOBs 121, 131, 141 and 151) can be coupled to receive the same clock signal.

[0018] Note that an external device attached to FPGA 100 must receive the input clock signal CLK_{IN}, and in response, generate clock signals equivalent to the CLK_0, CLK_{90}, CLK_{180} and CLK_{270} signals. The external device must have a first set of input circuits coupled to receive the equivalent CLK_0 signal, a second set of input circuits coupled to receive the equivalent CLK_{90} signal, a third set of input circuits coupled to receive the equivalent CLK_{180} signal, and a fourth set of input circuits coupled to receive the equivalent

CLK_{270} signal. The first, second, third and fourth sets of input circuits are coupled to receive the data signals clocked out of IOBs 121-124, 131-134, 141-144 and 151-154, respectively. The data values clocked out of IOBs 121-124, 131-134, 141-144 and 151-154 are then clocked into the first, second, third and fourth sets of input circuits of the external device in response to the equivalent CLK_0, CLK_{90}, CLK_{180} and CLK_{270} signals, respectively.

[0019] Fig. 3 is a circuit diagram illustrating a portion of a semiconductor chip 300 in accordance with another embodiment. In the described embodiment, semiconductor chip 300 is described as a programmable logic device, such as an FPGA (although this is not necessary). FPGA 300 and FPGA 100 include similar programmable logic resources.

[0020] The illustrated portion of FPGA 300 includes IOBs 301_0-301_N, DCM 311, programmable delay lines 321_1-321_N, delay select register 340 and arithmetic unit (AU) 350. DCM 311 includes delay select circuit 312, delay line 313 and multiplexer 314. Delay line 313 includes a plurality (X) of delay elements 315_1-315_X, which are connected in series as illustrated. The output terminals of delay elements 315_1-315_X are coupled to input terminals of multiplexer 314.

[0021] IOB 301_0 is configured to receive the CLK_0 signal from DCM 311. IOB 301_0 clocks the input signal IN_1 and output signal O_0 in response to the CLK_0 signal. As described in more detail below, the CLK_0 signal is synchronized with the input clock signal CLK_{IN}. In other embodiments, the CLK_0 can simply have a fixed phase relationship with respect to the CLK_{IN} signal.

[0022] The CLK_0 signal is propagated through delay lines 321_1-321_N, thereby creating delayed clock signals CLK_1-CLK_N, respectively. The delayed clock signals CLK_1-CLK_N are provided to IOBs 301_1-301_N, respectively. Thus, IOBs 301_1-

301_N, clock the respective input signals IN_1-IN_N and output signals O_1-O_N, in response to delayed clock signals CLK_1-CLK_N, respectively.

[0023] In the described embodiment, each of delay lines 321_1-321_N is programmed to introduce the same delay (although this is not necessary in all embodiments). The delay introduced by each of delay lines 321_1-321_N is selected in response to a delay control signal M provided by register 340. That is, the number of delay elements introduced by each of delay lines 321_1-321_N is selected in response to delay control signal M.

[0024] Fig. 4 is a circuit diagram of delay line 321_1 in accordance with one embodiment of the present invention. In this embodiment, delay line 321_1 includes series-connected delay elements 401_1-401_Z and multiplexer 402. The CLK_0 signal propagates through delay elements 401_1-401_Z, thereby creating delayed clock signals CD_1-CD_Z, respectively. The CLK_0 signal and the delayed clock signals CD_1-CD_Z are provided to input terminals of multiplexer 402. Delay control signal M is provided to control terminals of multiplexer 402. Multiplexer 402 routes one of the clock signals CLK_0, CD_1-CD_Z as the output clock signal CLK_1 in response to delay control signal M. For example, if the delay control signal M has a value of "3", then multiplexer 402 routes the clock signal CD_3 as the CLK_1 signal, thereby introducing three delay elements (and three delay periods) to the path of the CLK_0 signal. In this manner, delay control signal M controls the delay introduced by delay line 321_1. Each of delay elements 401_1-401_Z can be implemented by a plurality of series connected inverters, or by other well known delay circuitry. In the described this embodiment, delay lines 321_2-321_N are identical to delay line 321_1.

[0025] Returning now to Fig. 3, DCM 311 provides the CLK_0 signal in response to the input clock signal CLK_{IN}. More

specifically, the CLK_{IN} signal is applied to delay line 313. In response, delay elements 315_1-315_X provide delayed clock signals C_1-C_X, respectively. The CLK_{IN} signal and the delayed clock signals C_1-C_X are provided to input terminals of multiplexer 314. Delay select circuit 312, which is described in more detail below, provides delay select value Y to control terminals of multiplexer 314. Multiplexer 314 routes one of the clock signals CLK_{IN}, C_1-C_X as the output clock signal CLK_0 in response to delay select value Y.

[0026] The signal routed by multiplexer 314 is provided as the CLK_0 signal. As described above, the CLK_0 signal is provided to IOB 301_0 and delay line 321_1. The CLK_0 signal is also provided to an input terminal of delay select circuit 312 within DCM 311. Delay select circuit 312 compares the CLK_0 and CLK_{IN} signals, and adjusts the delay select value Y until the CLK_0 signal is synchronized with the CLK_{IN} signal. That is, delay select circuit 312 adjusts the delay select value Y until the delay introduced to the CLK_0 signal is equal to one period of the CLK_{IN} signal. The delay select value Y identifies the number of delay elements 315_1-315_X introduced to the path of the CLK_0 signal. Thus, when DCM 311 is locked, the delay select value Y identifies the number of delay elements 315_1-315_X corresponding with one period of the CLK_{IN} signal.

[0027] The number of delay elements (Z) in each of programmable delay lines 321_1-321_N is selected to be equal to a subset of the number of delay elements (X) in delay line 313. In one embodiment, delay line 313 includes 128 delay elements (i.e., X = 128), and each of programmable delay lines 321_1-321_N includes 8 delay elements (i.e., Z = 8). In one embodiment, the number N of delay lines coupled in series is selected such that the total number of delay elements in the series-connected delay lines 321_1-321_N equals the total

number of delay steps in delay line 313. Thus, in the described embodiment, N is equal to 16 (i.e., 128/8). Note that the variables Z, X and N can have other values in other embodiments.

[0028] Each of the delay elements in programmable delay lines 321_1-321_N is identical to the delay elements in delay line 313. For example, each of the delay elements 315_1-315_X in delay line 313 and each of the delay elements (e.g., 401_1-401_Z) in each of delay lines 321_1-321_N may introduce a signal delay of 200 picoseconds.

[0029] The delay select value Y is also provided to arithmetic unit 350. In response, arithmetic logic unit 350 divides the number of delay elements represented by delay select value Y by the number (N) of programmable delay elements 321_1-321_N, thereby creating a delay control value M that represents the number of delay elements to be inserted by each of the programmable delay lines 321_1-321_N. For example, if delay select value Y indicates that 42 delay elements (i.e., delay elements 315_1-315_{42}) are introduced to the path of the CLK_{IN} signal (i.e., the period of the CLK_{IN} signal is equal to 42 delay periods), then ALU 350 provides a delay control value M representative of the quotient of 42 and 16, or 2. Note that any fractional portion of the quotient is truncated. The delay control value M is stored in delay control register 340, and is provided to each of delay lines 321_1-321_N. In the described example, each of programmable delay elements 321_1-321_N introduces two delay periods in response to the delay control value M.

[0030] Fig. 5 is a waveform diagram illustrating the clock signals CLK_{IN}, CLK_0-CLK_{16} and associated data values (e.g., D1[16:0]) in accordance with the described embodiment. As shown in Fig. 5, the CLK_{IN} and CLK_0 signals exhibit rising edges at time T_0, and the CLK_1-CLK_{16} signals exhibit rising edges at times T_1-T_{16}, respectively. Delays of about 400

picoseconds (the delay associated with two delay elements) exist between the rising edges of the successive clock signals CLK_0-CLK_{16}.

[0031] As a result, the bits associated with data value D1 are sequentially switched out of IOBs 301_0-301_{16} in a "zipper-like" manner during a single cycle of the CLK_{IN} signal. Because these IOBs 301_0-301_{16} are not simultaneously switched, the transient output switching current is greatly reduced (e.g., by a factor of 17).

[0032] Although only one set of IOBs 301_0-301_N is illustrated in Fig. 3, it is understood that other identical sets of IOBs can be implemented in the same manner on the same FPGA.

[0033] When the temperature or other operating conditions of the FPGA change, the delay select value Y (i.e., the number of selected delay elements in delay line 313) may change dynamically. In this case, arithmetic logic unit 350 generates a new delay control value M (as appropriate) in response to the new delay select value Y. If a new delay control value M is generated (and stored in delay control register 340), then each of programmable delay lines 321_1-321_N is adjusted in view of this new delay control value M.

[0034] Although the invention has been described in connection with several embodiments, it is understood that this invention is not limited to the embodiments disclosed, but is capable of various modifications, which would be apparent to one of ordinary skill in the art. For example, the number of programmable delay line 321_1-321_N (Fig. 3) can be selected during configuration of the FPGA. That is, each IOB can have an associated programmable delay line that may be selectively coupled or de-coupled from adjacent programmable delay lines during the configuration of the FPGA. Thus, the present invention is only limited by the following claims.